NPN Darlington Power Transistor

Description

The ULN2001X is a monolithic high-voltage, high-current Darlington transistor array integrated circuit. It consists of three groups of NPN Darlington pairs, with its high-voltage output characteristics and cathode clamping diodes enabling the switching of inductive loads. The collector current for each Darlington pair is 250mA. Parallel connection of Darlington pairs allows for handling larger currents. This circuit is primarily used in relay drivers, hammer drivers, lamp drivers, display drivers (LED gas discharge), line drivers, and logic drivers.

Features

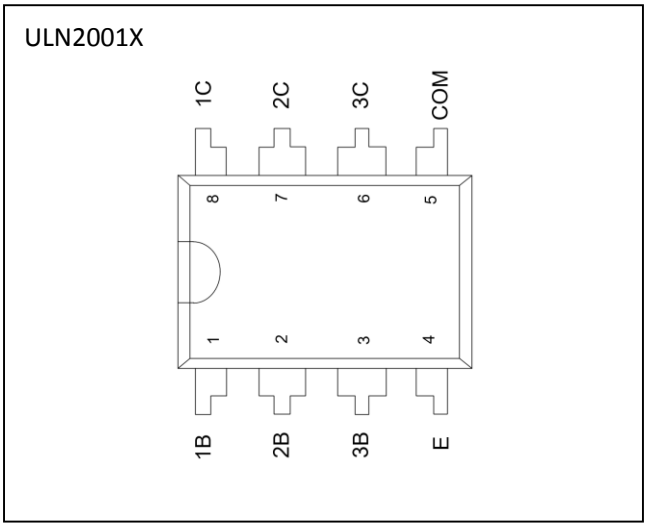
- Rated collector current: 250mA (per output)
- Maximum operating voltage: 50V
- Compatible with various logic types and inputs

Application

- Relay driver
- Hammer driver
- Lamp driver
- Logic driver

PINNING

ULN2001X



Model	Package
ULN2001I	DIP-8
ULN2001D	SOP-8
ULN2001Q	QIPAI-8

Absolute maximum ratings(TC=25)

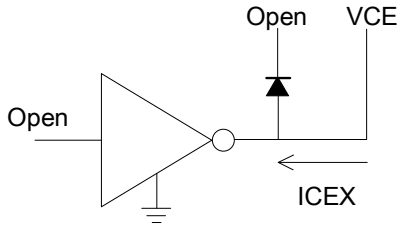
parameters	symbol	range	unit
Voltage between collector and emitter	V_{CE}	50	V
Input Voltage	V_I	30	V
Peak collector current	I_C	250	mA
Total transmitting current	IOK	1500	mA
power dissipation	Pd	950Tamb=25°C 495Tamb<85°C	mW
Working Temperature	Topr	-20～+85	°C
Storage temperature	Tstg	-65～+150	°C

Characteristic

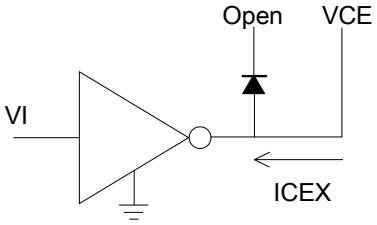
Tj=25 unless otherwise specified

parameter	trial	condition	min	type	max	unit
$V_{I(ON)}$ Input voltage	6	V_{CE}=2V， I_C=200mA			2.4	V
		V_{CE}=2V， I_C=250mA			2.7	
		V_{CE}=2V， I_C=300mA			3	
$V_{CE(SAT)}$ collector-emitter saturation voltage	5	I_I=250uA,I_C=100mA		0.9	1.1	V
		I_I=350uA,I_C=200mA		1	1.3	
		I_I=500uA,I_C=350mA		1.2	1.6	
I_{CEX} Collector cut-off current	1	V_{CE}=50V,I_I=0			50	uA
	2	V_{CE}=50V,I_I=0,Tamb=70°C			100	
V_F Forward clamp voltage	8	I_F =350mA		1.7	2	V
$I_{I(OFF)}$ Closed state output current	3	V_{CE}=50V,I_C=500mA,Tamb=70 °C	50	65		uA
I_I Input Current	4	VI=3.85V		0.95	1.35	mA
I_R Reverse clamping current	7	V_R =50V			50	uA
		V_R =50V, Tamb=70°C			100	
C_I Input capacitance	-	V_I=0, f=1MHz		15	25	pF
t_{PLH} Propagation delay time, low to high	9			0.25	1	us
t_{PHL} Propagation delay time, high to low	9			0.25	1	us
V_{OH} High level output	10	V_S=50V， I_O=300mA	V_S-20			mV

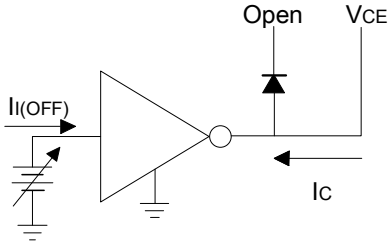
Test circuit diagram



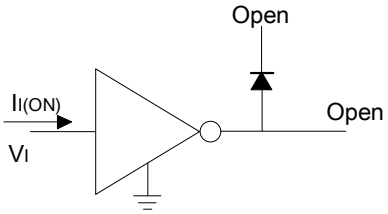
1 ICEX circuit diagram



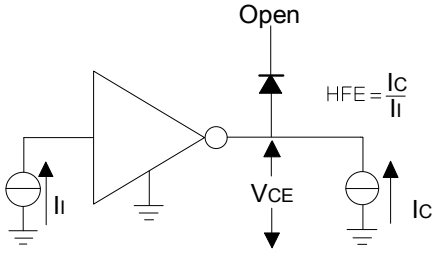
2 ICEX circuit diagram



3 $I_{I(OFF)}$ circuit diagram

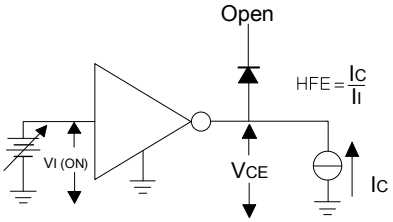


4 $I_{I(ON)}$ circuit diagram

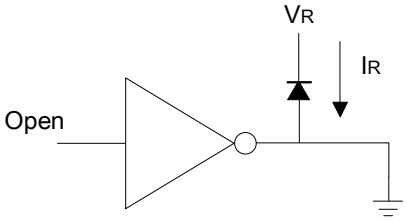


Note：II is a fixed measurement of VCE(SAT), it can also measure HFE

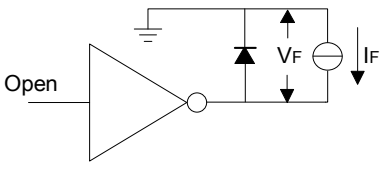
5 HFE，$V_{CE(SAT)}$ circuit diagram



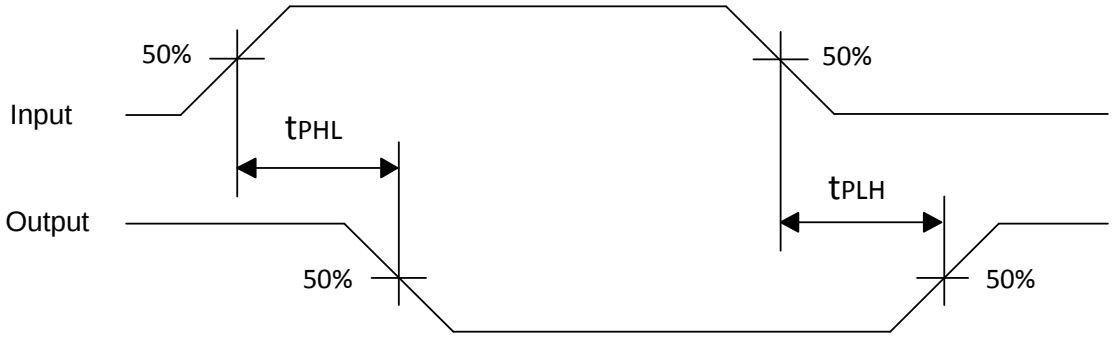
6 $V_{I(ON)}$circuit diagram



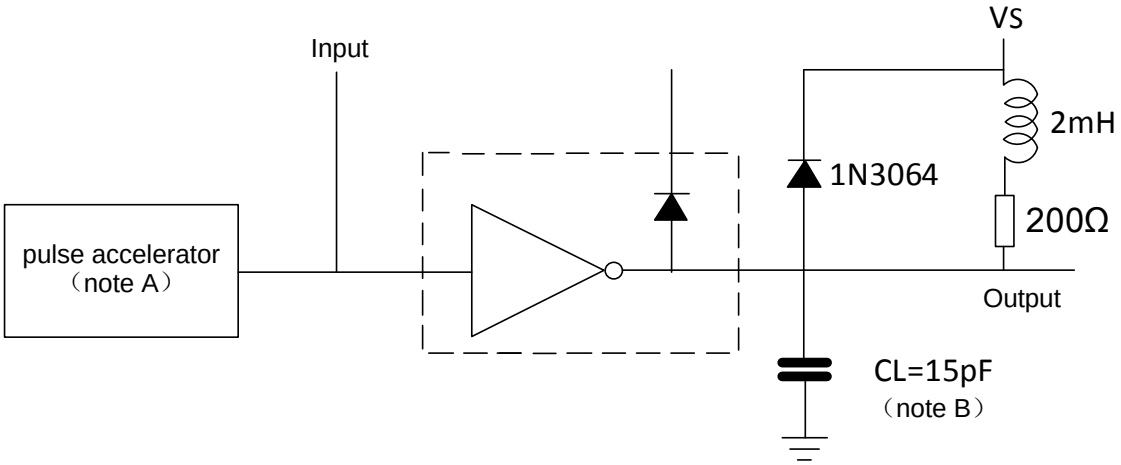
7 IR circuit diagram

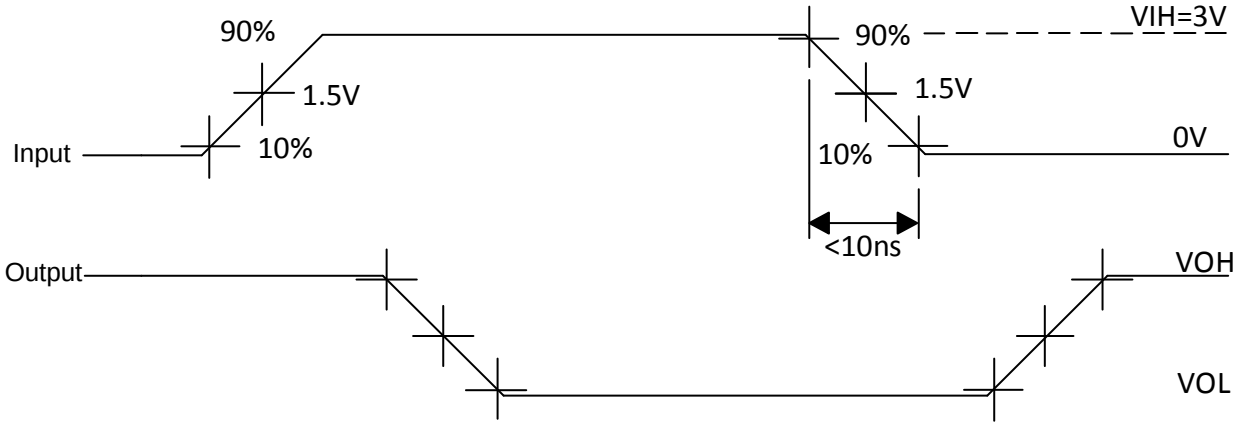


8 VF circuit diagram



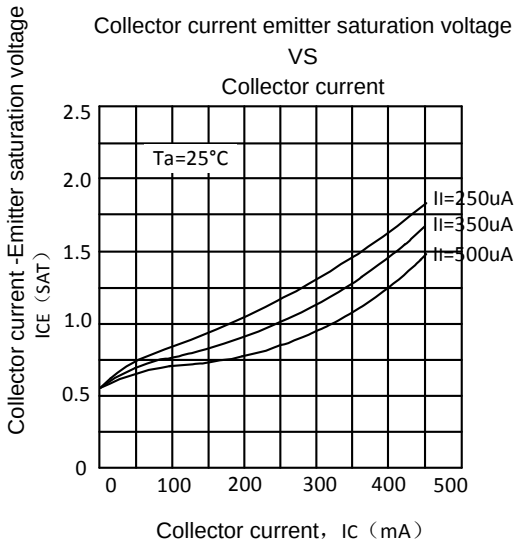
9 Propagation delay time waveform

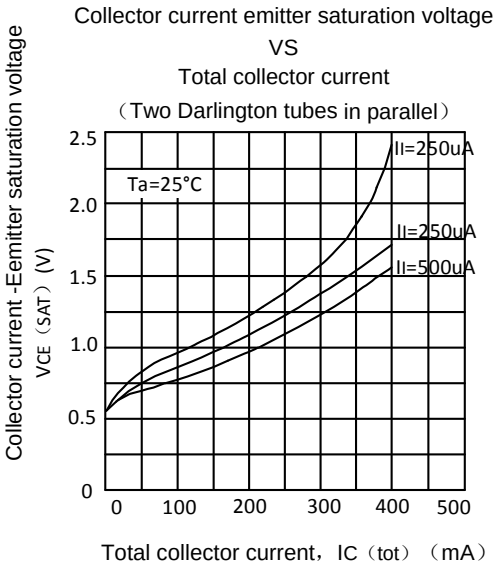


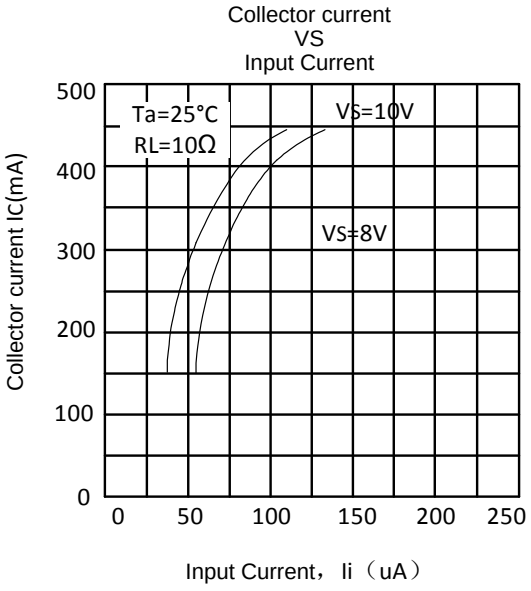


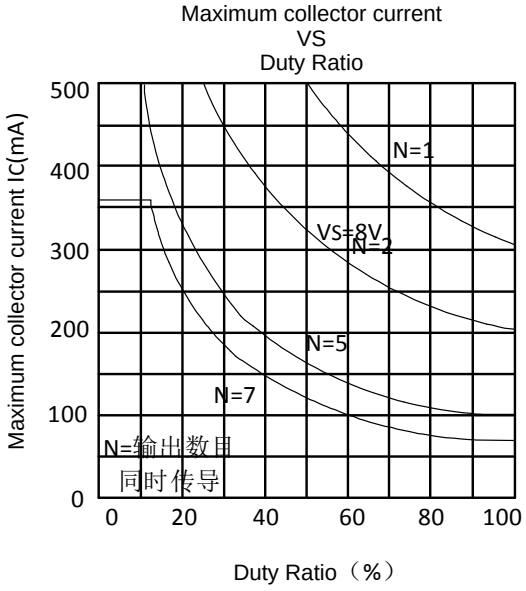
note：A.The pulse generator has the following characteristics：PRR=12.5kHz,Zo=50Ω
B.CLIncluding probes and mold capacitors

10 Latch test circuit diagram and voltage waveform


Collector current emitter saturation voltage
VS
Collector current
Collector current -Emitter saturation voltage
ICE（SAT）
Ta=25°C
II=250uA
II=350uA
II=500uA
2.5
2.0
1.5
1.0
0.5
0
0
100
200
300
400
500
Collector current，IC（mA）

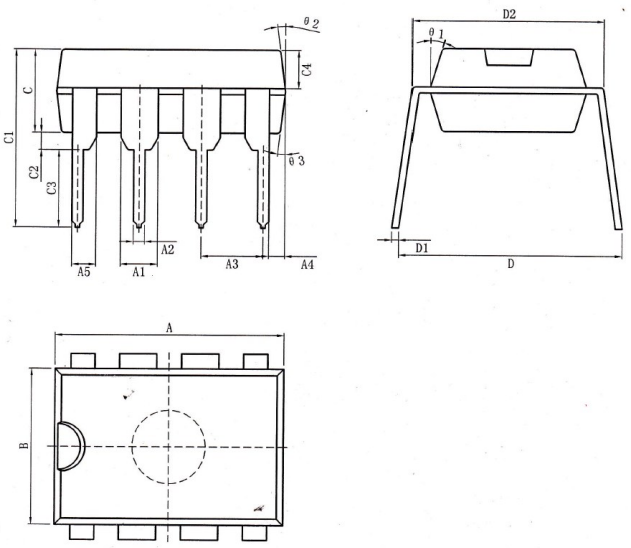

Collector current emitter saturation voltage
VS
Total collector current
（Two Darlington tubes in parallel）
Collector current -Eemitter saturation voltage
VCE（SAT）(V)
Ta=25°C
II=250uA
II=250uA
II=500uA
2.5
2.0
1.5
1.0
0.5
0
0
100
200
300
400
500
Total collector current，IC（tot）（mA）


Collector current
VS
Input Current
Collector current IC(mA)
Ta=25°C
RL=10Ω
VS=10V
VS=8V
500
400
300
200
100
0
0
50
100
150
200
250
Input Current，Ii（uA）


Maximum collector current
VS
Duty Ratio
Maximum collector current IC(mA)
N=1
VS=8V
N=2
N=5
N=7
N=输出数目
同时传导
500
400
300
200
100
0
0
20
40
60
80
100
Duty Ratio（%）

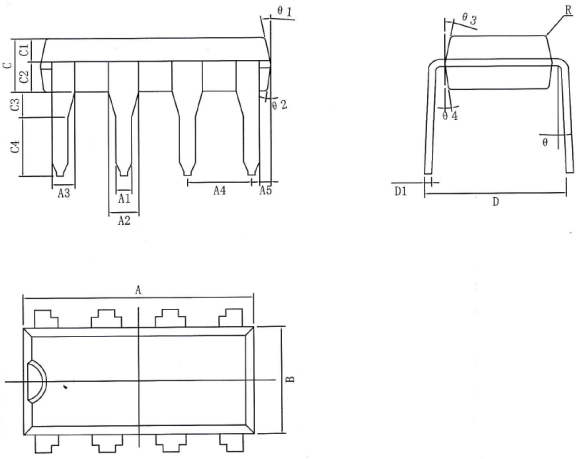
Configuration

1、DIP8



symbol	size (mm)	
	MIN	MAX
A	9.00	9.20
A1	1.474	1.574
A2	0.41	0.51
A3	2.44	2.64
A4	0.51TYP	
A5	0.99TYP	
B	6.10	6.30
C	3.20	3.40
C1	7.10	7.30
C2	0.50TYP	
C3	3.20	3.40
C4	1.47	1.57
D	8.20	8.80
D1	0.244	0.264
D2	7.62	7.87
Θ1	17°TYP	
Θ2	10°TYP	
Θ3	8°TYP	

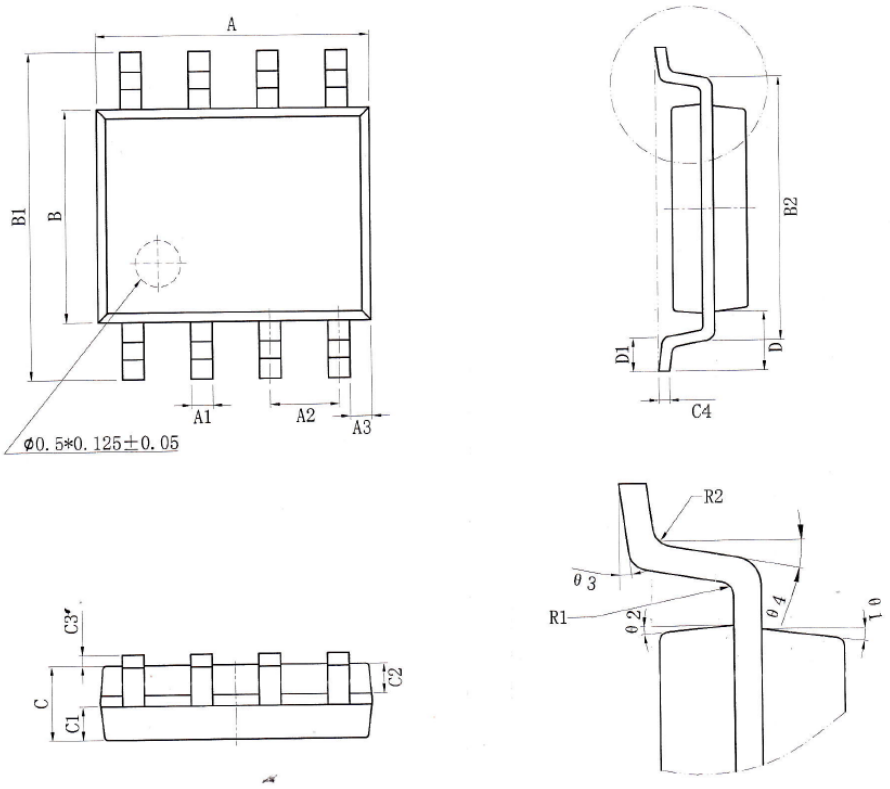
2、QIPAI8



symbol	size (mm)	
	MIN	MAX
A	6.45	6.55
A1	0.445	0.455
A2	0.845	0.855
A3	0.645	0.655
A4	1.75	1.85
A5	0.32	0.33
B	2.95	3.05
D	3.78	4.38
C	1.45	1.55
C1	0.60	0.70
C2	0.80	0.90
C3	0.65	0.75
C4	1.60	1.70
D1	0.195	0.205
Θ	2.5°TYP	
Θ1	12°TYP	
Θ2	8°TYP	
Θ3	12°TYP	
Θ4	8°TYP	
R	0.1TYP	

Configuration

3、SOP8



symbol	size (mm)		symbol	size (mm)	
	MIN	MAX		MIN	MAX
A	4.80	5.00	C4	0.203	0.233
A1	0.356	0.456	D	1.05TYP	
A2	1.27TYP		D1	0.40	0.80
A3	0.345TYP		D2	0.20TYP	
B	3.80	4.00	R1	0.20TYP	
B1	5.80	6.20	R2	0.20TYP	
B2	5.00TYP		Θ1	17°TYP	
C	1.30	1.60	Θ2	13°TYP	
C1	0.55	0.65	Θ3	0°~8°	
C2	0.55	0.65	Θ4	4°~12°	
C3	0.05	0.20			